

REMARKS

The Office Action mailed August 28, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

A "Petition for Extension of Time" for extending the due date for responding to the Office Action by one month and a credit card payment form to cover the fee payment (\$110.00) for the extension are filed with this Amendment. Authorization is granted to charge counsel's Deposit Account No. 01-2300, referencing **Attorney Docket No. 108066-00030**, for any additional fees necessary for entry of this Amendment.

The Specification and Figs. 1-2 and 5 have been amended. Claims 1, 3-4, 6, 8-11, and 13-17 have been amended. Applicants submit that the amendments made herein are fully supported in the Specification and the drawings, as originally filed, and therefore no new matter has been introduced. Accordingly, claims 1-17 are pending in the present application and are respectfully submitted for reconsideration.

Figs. 1-2 and 5 have been amended to correct typographical errors. Entry of these amendments is respectfully requested.

The Specification stands objected to for informalities. The objections are respectfully traversed. The Specification has been amended to correct typographical and grammatical errors in response to the Examiner's objections. Reconsideration is respectfully requested.

Claims 1-17 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Dependent claims 2-5 depend from independent claim 1, dependent claims 7 and 10 depend from independent claim 6 and dependent claims 12 and 16 depend from independent claim 11. Claims 1, 3, 6, 8, 10-11, 13 and 15-17 have been amended in response to the Examiner's rejections, and

it is submitted that the amended claims comply with 35 U.S.C. § 112, second paragraph. It is further submitted that dependent claims 2, 4-5, 7, 9, 12 and 14, rejected due to their dependence on rejected base claims, also comply with 35 U.S.C. § 112, second paragraph. The rejections are respectfully traversed and reconsideration is requested.

Claims 1-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yishay et al. patent (U.S. Patent No. 5,704,039) in view of the Akiyama et al. patent (U.S. Patent No. 5,784,464). Dependent claims 2-5, dependent claims 7-10 and dependent claims 12-16 depend from independent claims 1, 6 and 11, respectively. Claims 1, 4, 6, 9, 11, 14 and 17 have been amended. The rejections are respectfully traversed and reconsideration is requested.

The Yishay et al. patent discloses a security feature in which a data processing system 10 has a system integration circuit 16 connected to an external bus 28. In order to secure the internal memory of the data processor 10, a security circuit 42 is provided to the system integration circuit 16. This security circuit 42 has mask registers for storing accessible address and data, and compare circuit for comparing stored address and data and signals from the external bus 72 to protect an internal circuit. Further, the Yishay et al. patent discloses that the external bus is used for debug of the data processor.

The Akiyama et al. patent discloses a client authenticating system in which a server authenticates an access of the client. The server sends to registered client key (random number) to the access client and ciphers the client key. The client ciphers the received client key by the client own key and returns the ciphered key to the server. The server compares the received ciphered key and the ciphered client key to determine an authentication the access of the client.

Independent claim 1, as amended, recites an IC comprising an internal circuit; a debug I/F circuit for debugging the internal circuit externally; and an authentication circuit which is

provided between the debug I/F circuit and a debug terminal for connecting outside, and for transmitting a transmission key from the debug terminal to outside, and authenticating from a reception signal received from the debug terminal and the transmission key to enable operation of the debug I/F circuit, wherein the internal circuit comprises a CPU connected to the debug I/F circuit through a debug bus and a peripheral circuit connected to the CPU through an internal bus separated from the debug bus. Independent claim 6, as amended, recites an electronic device mounted with an IC, as claimed in claim 1. Independent claims 11 and 17, as amended, recite a debugging method and a debugger for debugging an IC, as claimed in claim 1, respectively. It is respectfully submitted that neither the Yishay et al. patent nor the Akiyama et al. patent, either alone or in alleged combination, discloses or suggests the IC, the electronic device mounted with an IC, the debugging method and the debugger for debugging an IC, as claimed in the present invention.

As acknowledged by the Examiner, the Yishay et al. patent "does not explicitly disclose transmitting a transmission key outside of the device, nor does Yishay explicitly disclose using the transmission key with the received signal to authenticate." The Examiner proceeds to rely on the Akiyama et al. patent as disclosing "a method for authenticating a client in which a transmission key is sent outside the authenticating device (column 11, lines 62-67) and authentication is performed by comparing the transmission key and a signal received from outside the authenticating device (column 12, lines 10-29)."

However, one of the unique features of the present invention is to prevent unfair access of the internal circuit through the debug exclusive use terminal (i.e., bus). More specifically, the Yishay et al. patent merely discloses preventing unfair access of the internal circuit through the normally used bus. The Yishay et al. patent fails to disclose or suggest an IC comprising, in

pertinent part, an internal circuit wherein the internal circuit comprises a CPU connected to the debug I/F circuit through a debug bus and a peripheral circuit connected to the CPU through an internal bus separated from the debug bus. Furthermore, the Yishay et al. patent fails to disclose or suggest that the authentication circuit which is provided between the debug I/F circuit and a debug terminal for connecting outside, as claimed in the present invention. Nor does the Akiyama et al. patent appear to disclose or suggest such a feature. Accordingly, both the Yishay et al. patent and the Akiyama et al. patent fail to disclose the invention, as claimed.

Since neither the Yishay et al. patent nor the Akiyama et al. patent discloses or suggests the IC, the electronic device mounted with the IC, the debugging method and the debugger, as claimed in the present invention, it is submitted that the alleged combination of these references also does not disclose or suggest the present invention as claimed. Nor even if the references were combinable, as suggested, would such alleged combination result in the claimed invention. It is therefore submitted that the references, either alone or in alleged combination, fail to disclose or suggest the present invention as claimed. Based upon the forgoing, it is respectfully submitted that independent claims 1, 6, 11 and 17 are patentable and in condition for allowance. Reconsideration is respectfully requested.

It is further submitted that dependent claims 2-5, dependent claims 7-10 and dependent claims 12-16 are also patentable and in condition for allowance due to their dependency upon independent claims 1, 6 and 11, respectively, since the dependent claims differ in scope from the corresponding parent claims. Dependent claims 2-5 depend from independent claim 1, dependent claims 7-10 depend from independent claim 6 and dependent claims 12-16 depend from independent claim 11, and thus are further limited to additional features of the invention. Therefore, it is respectfully submitted that the dependent claims are patentable over the alleged

combination of the Yishay et al. patent and the Akiyama et al. patent for at least the reasons set forth above with respect to independent claims 1, 6 and 11.

Dependent claims 4, 9 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yishay et al. patent in view of the Akiyama et al. patent and further in view of the Matsumura et al. patent (U.S. Patent No.4,908,038). The rejections are respectfully traversed and reconsideration is requested.

With reference to the above arguments concerning the independent claims, it is further submitted that the Yishay et al. patent, the Akiyama et al. patent and the Matsumura et al. patent, either each alone or in the alleged combination suggested by the Examiner in the Office Action, do not disclose or suggest the content of dependent claims 4, 9 and 14, which depend from independent claims 1, 6 and 11, respectively. As acknowledged by the Examiner, "neither the Yishay et al. patent nor the Akiyama et al. patent teach waiting a specified amount of time before enabling the operation of the debug interface." Nor does the Matsumura et al. patent directed to a high-security integrated-circuit (IC) card to prevent unauthorized use disclose or suggest the content of dependent claims 4, 9 and 14, namely, an IC wherein the authentication circuit time-waits the operation enabling after the authentication. Rather, the Matsumura et al. patent merely discloses an IC card security feature in which output of processing result is waited by a timer in order to make a processing time constant from receipt of the processing request to output of the processing result. Moreover, there is no suggestion to combine the references, as suggested by the Examiner in the Office Action. Nor even if the references were combinable, as suggested, would such alleged combination result in the claimed invention. It is therefore submitted that the dependent claims are also patentable and in condition for allowance.

Reconsideration is requested

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned counsel at the telephone number, indicated below, to arrange for an interview to expedite the disposition of this application.

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Respectfully submitted.



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FIG. 1

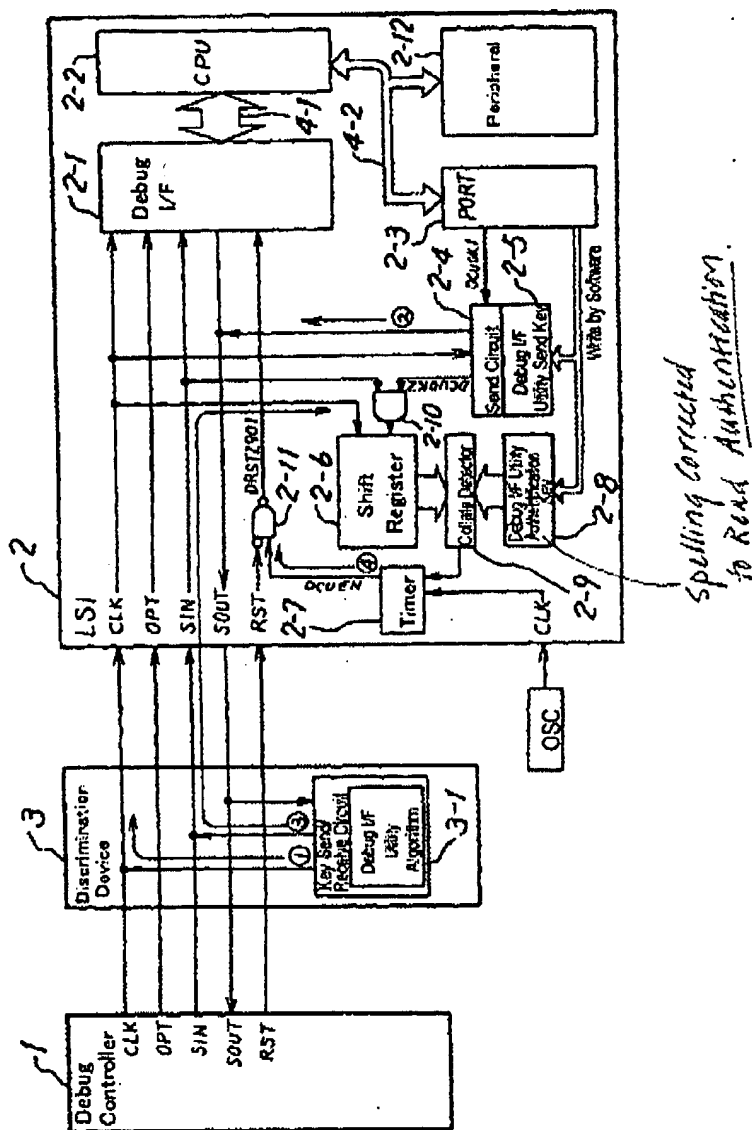


FIG. 2

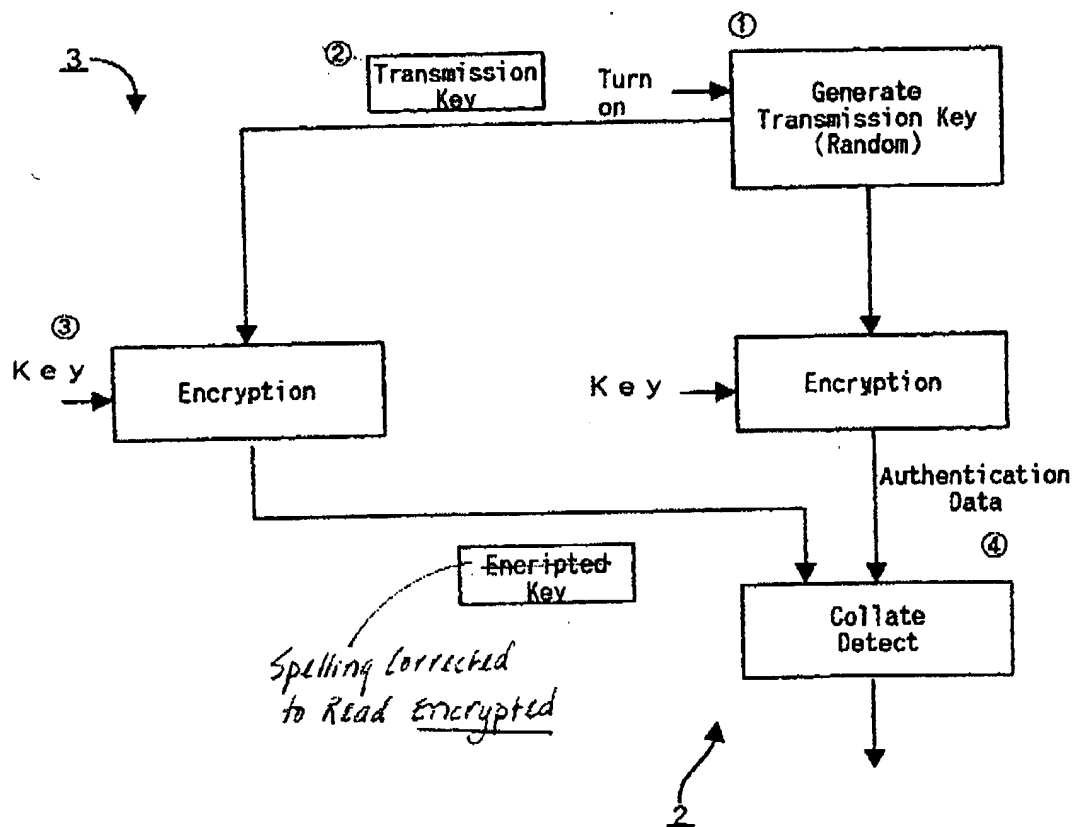
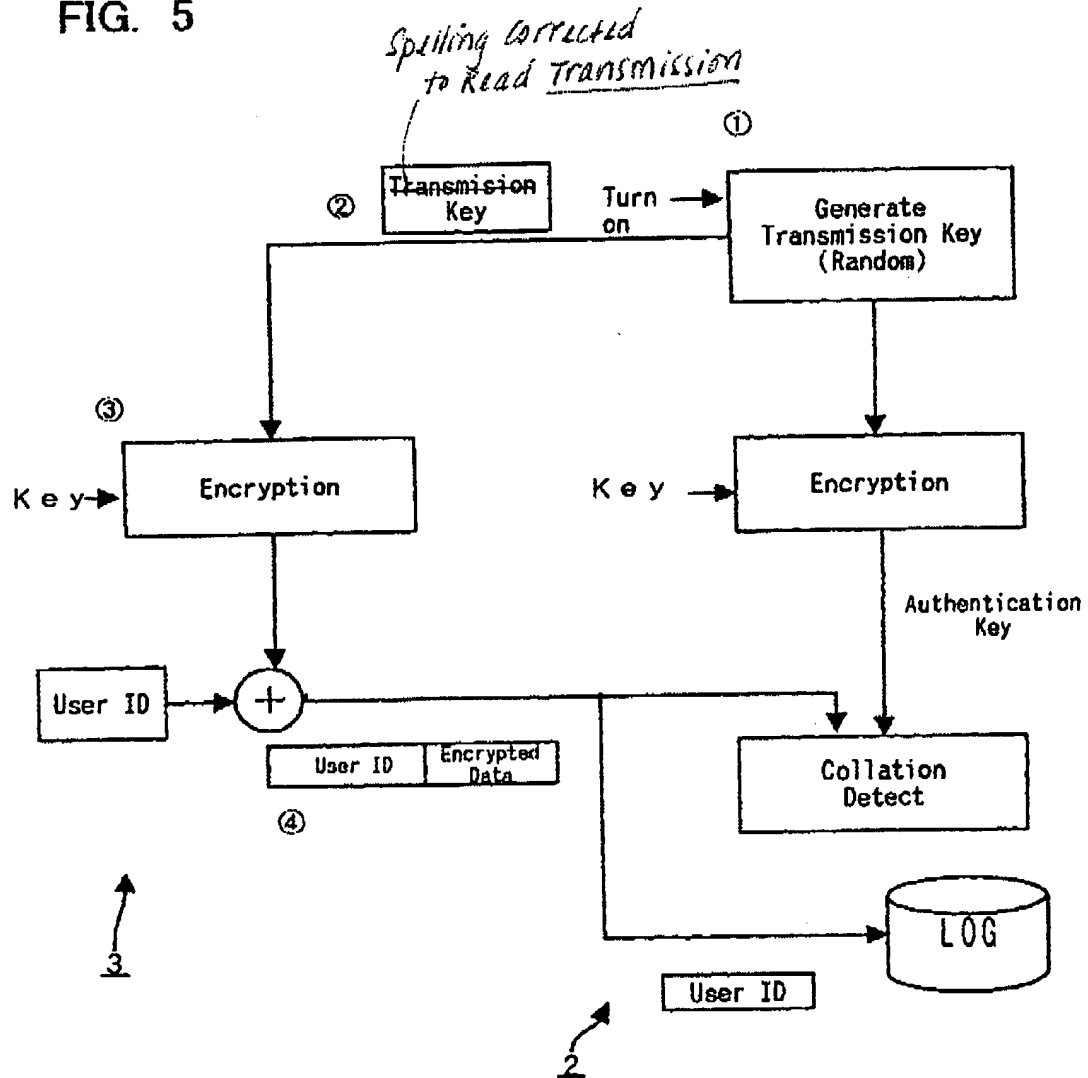


FIG. 5



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